REMARKS

Applicant thanks the Examiner for extending the courtesy of an interview to the applicant's representative on April 29, 2003.

Applicant has amended claims 1, 2, 4-8, and 10-16 in light of the discussions between the Examiner and applicant's representative and submits that all claims are allowable over the cited art. No new matter has been added. In particular, support for the subject matter claimed in claims 1, 2, 4-8, and 10-16 exists in the application at page 3, lines 18-24.

35 U.S.C. § 102

Claims 1-3, 7-9, and 13 stand rejected as allegedly anticipated by Fisher et al. (U.S. Patent No. 6,480,200). With respect to independent claims 1, 7, and 13, the Examiner asserts that Fisher discloses "a memory controller hub comprising: a graphics subsystem adapted to perform graphics operations on data (Fig. 1, Item No. 18); and a cache adapted to store addresses of locations in physical memory available to the graphics subsystem for storing graphics data (col. 1, lines 58-61) and available to the memory controller hub to store graphics data (Fig. 1, Item No. 18." Office action at 2-3.

The applicant disagrees because Fisher does not disclose a memory controller hub comprising a graphics subsystem. The graphics controller (Item No. 18) disclosed in Fisher is not part of the memory controller hub. Rather, it is an external component, connected to a memory controller hub by a bus. Applicant has amended claims 1, 7, and 13 to emphasize their patentable distinctions over the cited art. Because Fisher does not disclose a memory controller hub comprising an internal graphics subsystem, Fisher does not anticipate the claims. Claims 2-3 depend from claim 1, and are patentable for at least the same reasons that claim 1 is patentable. Claims 8-9 depend from claim 7, and are patentable for at least the same reasons that claim 7 is patentable.

35 U.S.C. § 103

Claims 4-6, 10-12, and 14-16 stand rejected as allegedly obvious over Fisher et al. in view of Surti (U.S. Patent No. 6,496,193). The Examiner asserts that "Fisher et al further disclose a cache adapted to store addresses of locations in physical memory (col. 1, lines 58-61)" and that "Surti et al disclosed a method and apparatus for fast loading of texture data into tile memory, wherein texture data are store [sic] in system memory in a tile format that allows an entire cache tile to be stored linearly in memory space (col. 2, lines 8-10; col. 4, lines 3-5, 47-51)." Office action at 4.

Applicant respectfully traverses this rejection. Claims 4-6 depend from claim 1, and are patentable for at least the same reasons that claim 1 is patentable (see above). Claims 10-12 depend from claim 7, and are patentable for at least the same reasons that claim 7 is patentable (see above). Claims 14-16 depend from claim 13, and are patentable for at least the same reasons that claim 7 is patentable (see above).

The absence of a response to any particular position of the Examiner should not be construed as a concession by the applicant of any such position. The expression of a response by the applicant should not be construed as a concession that there are not other reasons for patentability.